CLAIM(S)

1. A clock management system, comprising:

a controller;

a bus interface, the bus interface further comprising a bus clocking signal and a bus activity signal;

a plurality of oscillators, each oscillator operating at unique clock speeds; and

selection means for operatively coupling to the controller one of the group consisting of the plurality of oscillators and the bus clocking signal;

wherein upon receipt of a bus activity signal the selection means selects the bus clocking signal, otherwise the selection means selects the oscillator with the lowest frequency necessary for the controller to operate.

2. The clock management system of claim 1 wherein the controller operates the selection means.

3. The clock management system of claim 1 wherein each of the plurality of oscillators operates in one of a power off mode and a power on mode, the controller being operatively coupled to each oscillator causing each oscillator to operate in the power on mode only when selected by the selection means.

4. The clock management system of claim 1 further comprising a wireless interface operatively coupled to the controller.

5. The clock management system of claim 4 wherein the controller having a sleep mode, the controller synchronizing the time period for the sleep mode with the wireless interface.

6. A clock management system, comprising:

a Media Access Controller;

a high frequency oscillator;

a low frequency oscillator;

a bus interface for a bus selected from the group consisting of a PCI bus and Cardbus, the bus interface having a bus clock and a wakeup signal connection;

selection means for selecting one of the high frequency oscillator, low frequency oscillator, and bus clock to be used for clocking the Media Access Controller;

wherein the bus interface wakeup signal connection is directly connected to the Media Access Controller, the Media Access Controller controls the selection means, and the Media Access Controller controls the operating mode of the high frequency oscillator.

7. The clock management system of claim 6 wherein the Media Access Controller is 802.11 compliant.

8. The clock management system of claim 6 wherein the high frequency oscillator is turned off when not in use by the Media Access Controller.

9. The clock management system of claim 6 wherein a signal from the bus interface wakeup signal causes the selection means to select the bus clock.

10 The clock management system of claim 6 wherein the Media Access Controller enters into a sleep mode for a predetermined time, wherein the selection means selects the low frequency clock and the high frequency oscillator is turned off during the sleep mode.

11 The clock management system of claim 10 wherein the Media Access Controller causes the high frequency oscillator to begin operation and the selection means to select the high frequency clock upon exiting the sleep mode.

12. The clock management system of claim 11 wherein a signal on the wakeup signal connection causes the Media Access Controller to change from sleep mode to an awake mode prior to the completion of the predetermined time period and the Media Access Controller causes the selection means to select the bus clock.

13. The clock management system of claim 6 wherein the selection means is a

multiplexer.

14. A method for managing a clock management system for a controller having a sleep mode, an active mode and a sleep mode timer, comprising the steps of:

providing a high frequency oscillator, a low frequency oscillator and a controllable selection means for selecting one of the high frequency and low frequency oscillator;

operating the controller with the low frequency oscillator while in sleep mode;

enabling the high frequency oscillator upon expiration of the sleep mode timer;

switching the controller to the frequency oscillator when the high frequency oscillator becomes fully operational;

switching the controller to active mode;

processing transactions by the controller;

switching to the low frequency controller;

resetting the sleep mode timer;

disabling the high frequency oscillator; and

switching to sleep mode;

15. The method for managing a clock management system as in claim 14 further comprising:

waiting for a DTIM beacon while the controller is in active mode; and

receiving data traffic

16. The method for managing a clock management system as in claim 14 further comprising

providing a bus interface clock signal to the controllable selection means and a bus interface wakeup signal connection to the controller, wherein the controllable selection means selects one of the high frequency oscilliator, the low frequency oscillator and the interface clock signal;

sending a bus interface wakeup signal to the controller;

commanding the selection means to switch to the interface clock signal; and

switching the selection means to the interface clock signal.

17. A clock management system, comprising:

a plurality of clocking means, each clocking means operative at a specific frequency;

selection means receiving inputs from the plurality of clocking means;

controller means for selecting one of the plurality of clocking means

enabling means connected to at least one of the plurality of clocking means for the

wherein the controller means operates to cause the selection means to select the clocking with the lowest frequency necessary for the controller meansto operate; and

wherein the enabling means turns off the at least one of the plurality of clocking means when it is not the clocking means selected by the selection means.

18. A controller having a computer readable medium with computer readable instructions stored thereon, the controller receiving a clocking signals from a selection means, the selection means receiving a high frequency clocking signal from a high frequency oscillator, a low frequency signal from a low frequency oscillator, the controller selecting of the high frequency signal, low frequency signal from the selection means, the controller further having enabling means for powering on and powering off the high frequency oscillator, the computer readable instructions comprising:

computer readable instruction means for setting a timer;

computer readable instructions for causing the selection means to select the low frequency signal;

computer readable instruction means for powering off the high frequency oscillator;

computer readable instructions responsive to the timer for powering on the high frequency oscillator after the timer expires; and

computer readable instructions for causing the selection means to select the high frequency clock signal after the high frequency oscillator achieves normal operating condition.

19. A controller as in claim 18 wherein the selection means further comprises an input from a bus interface having a bus clocking signal wherein the controller selects one of the high frequency signal, low frequency signal and bus clocking signal, the controller further comprising a bus signaling means received from the bus interface, the computer readable instructions further comprising computer readable instructions responsive to the bus signaling means for:

receiving a wakeup signal from the bus signaling means;

commanding the selection means to select the bus clocking signal;

processing an instruction from the bus; and

commanding the selection means to select the low frequency signal.

receiving data from the wireless interface;

commanding the selection means to select the low frequency signal after receiving data from the wireless interface.

20. The controller as in claim 19 wherein the controller further comprises a wireless interface, further comprising computer readable instructions operative only when the selection means has selected the high frequency signal for:

waiting for the wireless interface to receive a TIM beacon;

receiving data from the wireless interface;

commanding the selection means to select the low frequency signal after receiving data from the wireless interface.